MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Reconfigurable Computing Systems**			**Module Delivery**	
Module Type	**Elective**			☒ **Theory** ☐ **Lecture** ☒ **Lab** ☐ **Tutorial** ☐ **Practical** ☒ **Seminar**	
Module Code	**CET4206**				
ECTS Credits	**5**				
SWL (hr/sem)	**150**				
Module Level	4		**Semester of Delivery**	8	
Administering Department	CET		**College**	EETC	
Module Leader	Dr. Mohanad Ahmed Mezher		**e-mail**	mohanad.ahmed1@mtu.edu.iq	
Module Leader's Acad. Title	Professor		**Module Leader's Qualification**	M.Sc	
Module Tutor	Siraj Qays Mahdi		**e-mail**	Siraj_qays@mtu.edu.iq	
Peer Reviewer Name	Dr. Osama Abbas Hussein		**e-mail**	osama.abbas@mtu.edu.iq	
Scientific Committee Approval Date	13/06/2023		**Version Number**	1.0	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Aims أهداف المادة الدراسية	1. Understand the fundamentals of the reconfigurable computing and reconfigurable architectures 2. Articulate the design issues involved in reconfigurable computing systems with a specific focus on Field Programmable Gate Arrays (FPGAs) both in theoretical and application levels 3. Understand the performance trade-offs involved in designing a reconfigurable computing platform with a specific focus on the architecture of a configurable logic block and the programmable interconnect 4. Discuss the state-of-the-art reconfigurable computing architectures spanning fine grained (look up table-based processing elements) to coarse grained (arithmetic logic unit level processing elements) architectures. 5. Understand both how to architect reconfigurable systems and how to utilize them for solving challenging computational problems.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. an ability to apply knowledge of mathematics, science, and engineering (High) 2. an ability to design and conduct experiments, as well as to analyze and interpret data (High) 3. an ability to design a system, component, or process to meet desired needs within realistic constraints (High) 4. an ability to identify, formulate, and solve engineering problems (High) 5. an ability to communicate effectively (Medium) 6. a recognition of the need for, and an ability to engage in life-long learning (Medium) 7. a knowledge of contemporary issues (High) 8. an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice. (High)
Indicative Contents المحتويات الإرشادية	--Introduction to Reconfigurable Computing (5 hr) --FPGA Architectures(10 hr) --FPGA Design Cycle (20 hr) --Coarse-grained Reconfigurable Devices (10 hr) --Reconfigurable Computing Applications (7 hr) --Multi-FPGA Systems (5 hr) --FPGAs vs. Multicore architectures (5 hr) --Advanced Topics (12 hr)

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	Type something like: The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, interactive tutorials and by considering type of simple experiments involving some sampling activities that are interesting to the students.

Student Workload (SWL) الحمل الدراسي للطالب			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	74	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	5
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	76	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	5
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	150		

Module Evaluation تقييم المادة الدراسية					
		Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**
Formative assessment	**Quizzes**	2	10% (10)	5, 10	LO #1, 2, 10 and 11
	Assignments	2	10% (10)	2, 12	LO # 3, 4, 6 and 7
	Projects / Lab.	1	10% (10)	Continuous	
	Report	1	10% (10)	13	LO # 5, 8 and 10
Summative assessment	**Midterm Exam**	2 hr	10% (10)	7	LO # 1-7
	Final Exam	4hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري	
	Material Covered
Week 1	Introduction to Reconfigurable Computing
Week 2-3	FPGA Architectures
Week 4-7	FPGA Design Cycle • Technology-independent optimization • Technology Mapping • Placement • Routing
Week 8-9	Coarse-grained Reconfigurable Devices
Week 11	Reconfigurable Computing Applications
Week 12	Multi-FPGA Systems
Week 13	FPGAs vs. Multicore architectures
Week 14-15	Advanced Topics: • Dynamic Reconfiguration • Partial Reconfiguration • 3D FPGAs

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Lab 1: Introduction to ISE design suite software
Week 2	Lab 2: VHDL programming tools
Week 3	Lab 3: programming simple VHDL program
Week 4	Lab 4: IF statements -VHDL programs
Week 5	Lab 5: For loop -VHDL programs
Week 6	Lab 6: UP-Down counters
Week 7	Lab 7: Multi functions programs

Learning and Teaching Resources مصادر التعلم والتدريس		
	Text	**Available in the Library?**
Required Texts	: (Optional) Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation by Scott Hauck, André DeHon.	Yes
Recommended Texts	C. Maxfield, The Design Warrior's Guide to FPGAs, Newnes, 2004, ISBN: 978-0750676045	No
Websites	http://class.ece.iastate.edu/cpre583/	

Grading Scheme مخطط الدرجات				
Group	**Grade**	التقدير	**Marks (%)**	**Definition**
Success Group (50 - 100)	**A -** Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX –** Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.