MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Advanced Computer Technology**			**Module Delivery**	
Module Type	Core			☒ **Theory** ☐ **Lecture** ☒ **Lab** ☐ **Tutorial** ☐ **Practical** ☐ **Seminar**	
Module Code	**CET4202**				
ECTS Credits	**5**				
SWL (hr/sem)	**150**				
Module Level	4		**Semester of Delivery**	8	
Administering Department	CET		**College**	EETC	
Module Leader	Dalal Abdulmohsin Hammood		**e-mail**	dalal.Hammood@mtu.edu.iq	
Module Leader's Acad. Title	Professor		**Module Leader's Qualification**	Ph.D.	
Module Tutor	Prof. Dr. Mahmood Farhan Mosleh		**e-mail**	drmahmood@mtu.edu.iq	
Peer Reviewer Name	Dr. Mahmoud Shuker Mahmoud		**e-mail**	mahmoud.shukur@mtu.edu.iq	
Scientific Committee Approval Date	13/06/2023		**Version Number**	1.0	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Aims أهداف المادة الدراسية	The course aims to provide students information about : 1. The µP and its architecture and the addressing modes 2. Paging mechanism, Segment translation and Page translation 3 Cache memory, Cache organization, fully associative, Direct mapped and Set associative 4. Cache memory used for 80386 - Direct Maps - Two-way set associative 5. Intel's Pentium and its Features 6. Pentium pro, Out of order execution 7. other Pentium processors, Core processor
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1- an ability to apply knowledge of microprocessor Architecture. (High) 2- an ability to apply knowledge about 80386 The µP (High) 3- an ability to apply knowledge about Paging mechanism, Segment translation and Page translation (High) 4- an ability to identify and calculate the addressing mode and physical address (High) 5- an ability to calculate the data and tag for cache (High)
Indicative Contents المحتويات الإرشادية	**-Introduction to the Microprocessor and Computer (5 hr)** **-The µP 80386 architecture (14 hr)** **-Protected mode memory addressing (10hr)** **-Descriptor and page table entries(10 hr)** **-Memory paging(10 hr)** **-Paging mechanism(5 hr)** **-A translation lookaside buffer (TLB) (10hr)** **-Cache memory(10 hr)** **-Intel's Pentium(5 hr)**

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	Type something like: The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, interactive tutorials and by considering type of simple experiments involving some sampling activities that are interesting to the students.

Student Workload (SWL) الحمل الدراسي للطالب			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	74	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	5.2
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	76	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	5.4
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	150		

Module Evaluation
تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	Quizzes	2	10% (10)	5, 10	LO #1-4
	Assignments	2	10% (10)	2, 12	LO # 1-4
	Projects / Lab.	1	10% (10)	Continuous	
	Report	1	10% (10)	13	LO # 1-4
Summative assessment	Midterm Exam	2 hr	10% (10)	7	LO # 1,2
	Final Exam	4hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري	
	Material Covered
Week 1	**Introduction to the Microprocessor and Computer**
Week 2	**The μ_p 80x86 and its architecture** **Internal organization of μ_p 80x86**
Week 3-4	**The μ_P 80386 architecture** • **Addressing mode** • **Assembly language** **Memory segmentation**
Week 5-6	**Protected mode memory addressing** • **Selectors and descriptors** • **Local and global descriptors tables**
Week 7	**Descriptor and page table entries** • **Program-invisible registers** • **Illustrating local memory access.** **Examples**
Week 8-9	**Memory paging** **Virtual memory**
Week 10	**Paging mechanism** • **Segment translation** • **Page translation**
Week 11	**A translation lookaside buffer (TLB)** **Examples**
Week 12	**Major changes in the 80386 μ_p**
Week 13	**Cache memory** • **Cache organization** • **Fully associative** • **Direct mapped** **Set associative**
Week 14	**Cache memory used for 80386** • **Direct Maps** • **Two-way set associative**
Week 15	**Intel's Pentium** • **Features of the Pentium** **Intel's overdrive technology**

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Lab 1: Introduction to Mp 80386
Week 2	Lab 2: programming using assembly language
Week 3	Lab 3: programming many functions
Week 4	Lab 4: programming many functions using Assembly Language
Week 5	Lab 5: Examples
Week 6	Lab 6: Examples
Week 7	Lab 7: Examples

Learning and Teaching Resources مصادر التعلم والتدريس		
	Text	**Available in the Library?**
Required Texts	The 80x86 IBM Pc and compatible computer	Yes
Recommended Texts		No
Websites		

Grading Scheme مخطط الدرجات				
Group	**Grade**	التقدير	**Marks (%)**	**Definition**
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.