MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية			
Module Title	**Microprocessors**	**Module Delivery**	
Module Type	**Core**	☒ Theory ☐ Lecture ☒ Lab ☒ Tutorial ☐ Practical ☐ Seminar	
Module Code	**CET2203**		
ECTS Credits	**6**		
SWL (hr/sem)	**180**		
Module Level	2	**Semester of Delivery**	4
Administering Department	CET	**College**	EETC
Module Leader	Aseel Hameed Majeed	**e-mail**	Aseel_Alnakkash@mtu.edu.iq
Module Leader's Acad. Title	Ass. Professor	**Module Leader's Qualification**	Ph.D.
Module Tutor	Dr. Dalal Abdulmohsin Hammood	**e-mail**	dalal.Hammood@mtu.edu.iq
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Scientific Committee Approval Date	10/06/2023	**Version Number**	1.0

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	Computer Organization & Architecture (CET2103)	**Semester**	3
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Aims أهداف المادة الدراسية	1. To understand the basic operating concept of specific microprocessor. 2. To study the hardware architecture of specific microprocessor. 3. To encode programs based on the specific processor language. 4. To solve problems encountered in the architecture of a specific microprocessor
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Identify the basic characteristic of specific processor 2. Define the processor signals and their functions 3. Explain the architecture from the hardware point of view 4. Identify various machine cycle. 5. Explain the memory different interfacing techniques with the microprocessor. 6. Explain the input output different interfacing techniques with the microprocessor. 7. Explain the concept of Stack memory. 8. List the addressing mode of the processor instruction. 9. Encode different program based on assembly. 10. Perform different arithmetic and logical operations using the processor instruction set. 11. Encode different problems associative with branching instructions. 12. Solve problem encountered with delay and counter. 13. Identify different interrupt procedures. 14. Design different interfacing systems due to the problem requirements.
Indicative Contents المحتويات الإرشادية	Indicative content includes the following. <u>Part A – Microprocessor H/W architecture</u> --MP signals, MP operations, Machine cycle, memory interfacing, input-output devices interfaces [30hrs] <u>Part b – Microprocessor S/W architecture</u> --Instruction set, data transfer, arithmetic, logical. [25 hrs] --Stack register and stack area [15hrs] --Branching instructions and applications [20hrs] --Revision problem classes [10 hrs]

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, interactive tutorials and by considering type of simple experiments involving some sampling activities that are interesting to the students.

Student Workload (SWL) الحمل الدراسي للطالب			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	102	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	7.2
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	78	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	5.57
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	180		

Module Evaluation
تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	Quizzes	2	10% (10)	7, 10	LO #1- 6, LO #8-11
	Assignments	5	10% (10)	Continuous	
	Projects / Lab.	5	10% (10)	Continuous	
	Report	2	10% (10)	7,10	LO #1- 6, LO # 8-11
Summative assessment	Midterm Exam	2 hr	10% (10)	7	LO # 1-7
	Final Exam	4hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري	
	Material Covered
Week 1	Introduction - microprocessor evolution
Week 2	Basics specific microprocessor architecture and its specifications
Week 3	Microprocessor signals and machine cycle
Week 4	Memory organization, interfacing and memory map
Week 5	Input devices interfacing
Week 6	Output devices interfacing
Week 7	Introduction to microprocessor assembly language and addressing mode
Week 8	Data transfer instruction
Week 9	Arithmetic instructions
Week 10	logical instruction
Week 11	Stack register , stack area and related instructions
Week 12	Branching instruction
Week 13	Delay and counters
Week 14	Interrupt concept and types
Week 15	**Subroutine**
Week 16	**Preparatory week before the final Exam**

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Lab 1: Introduction to microprocessor kit
Week 2	Lab 2: key function definition, read/write memory location, read/write registers
Week 3	Lab 3: Data transfer instructions
Week 4	Lab 4: Arithmetic instructions
Week 5	Lab 5: logical instruction
Week 6	Lab 6: Stack instructions
Week 7	Lab 7: Branching instruction

Learning and Teaching Resources مصادر التعلم والتدريس		
	Text	**Available in the Library?**
Required Texts	8085 µp architecture and programming_Gonkar	Yes
Recommended Texts	UNDERSTANDING 8085/8086 MICROPROCESSORS and PERIPHERAL ICs	no
Websites	https://www.coursera.org/browse/physical-science-and-engineering/electrical-engineering	

Grading Scheme مخطط الدرجات				
Group	**Grade**	التقدير	**Marks (%)**	**Definition**
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.