MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	Microcontroller			**Module Delivery**	
Module Type	C			☒ Theory ☐ Lecture ☒ Lab ☐ Tutorial ☐ Practical ☐ Seminar	
Module Code	ATU11611				
ECTS Credits	6				
SWL (hr/sem)	150				
Module Level	UGIII		**Semester of Delivery**	2	
Administering Department			**College**	NETC	
Module Leader			**e-mail**		
Module Leader's Acad. Title			**Module Leader's Qualification**		
Module Tutor	Name (if available)		**e-mail**		
Peer Reviewer Name	Nasir Hussein Selman		**e-mail**	Coj.nas@atu.edu.iq	
Scientific Committee Approval Date	01/05/2025		**Version Number**	1.0	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	1- Understand FPGA Fundamentals and provide students with a comprehensive understanding of FPGA technology, including its definition, historical development, and various applications. 2- To familiarize students with the basic components and structure of FPGAs, including LUTs, flip-flops, registers, multiplexers, CLBs, I/O blocks, and interconnects. 3- To introduce students to VHDL as a hardware description language, including design flow, EDA tools, and translating VHDL code into circuit implementations. 4- Design Digital Systems by providing practical experience in designing digital systems such as Multiply Accumulate Circuits (MAC), digital filters, and neural networks using VHDL and FPGA. 5- Integrate MATLAB with FPGA to explore the integration of MATLAB with FPGAs for system design and simulation purposes.

Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Describe the fundamental concepts of FPGA technology and its applications in various fields. 2. Identify and explain the components of FPGA architecture and their functions. 3- Write basic VHDL code and implement both parallel and sequential VHDL code, including FSMs for digital design. 6. Design and simulate digital circuits such as MAC and digital filters using VHDL on an FPGA platform. 7. Utilize MATLAB for modeling and simulating FPGA designs effectively.
Indicative Contents المحتويات الإرشادية	1. FPGA Overview & architecture 2. Logic circuit application using VHDL 3. FPGA with MATLAB

Learning and Teaching Strategies
استراتيجيات التعلم والتعليم

Strategies	The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, interactive tutorials and by considering types of simple experiments involving some sampling activities that are interesting to the students.

Student Workload (SWL)
الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا

Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	78	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	72	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	**150**		

Module Evaluation
تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	**Quizzes**	2	10% (10)	5 and 10	LO #1, #2 and #10, #11
	Assignments	2	10% (10)	2 and 12	LO #3, #4 and #6, #7
	Projects / Lab.	1	10% (10)	Continuous	All
	Report	1	10% (10)	13	LO #5, #8 and #10
Summative assessment	**Midterm Exam**	2hr	10% (10)	7	LO #1 - #7
	Final Exam	3hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)
المنهاج الاسبوعي النظري

	Material Covered
Week 1	**Overview of FPGA**: Definition, History, and Applications - FPGA vs ASIC: Differences and use cases - FPGA architecture: Basic Components and Structure - Look-up tables (LUT) - Flip-flops, Registers, and Multiplexers - CLBs (Configurable Logic Blocks) - I/O Blocks and Interconnects
Week 2	About VHDL - Design Flow - EDA Tools - Translation of VHDL Code into a Circuit
Week 3	Fundamental VHDL Units- LIBRARY Declarations- Entity Declaration - Architecture body - Behavioral model
Week 4	VHDL Data Types - VHDL Data Classes
Week 5	VHDL Parallel Code
Week 6	VHDL for Sequential code inside Processes
Week 7	Finite State Machines (FSM)
Week 8	Arithmetic Logic Elements- Logic Implementation Using FPGA
Week 9	Packages and Components
Week 10	**Mid-Term Exam**
Week 11	Function and Procedure
Week 12	System Design Multiply Accumulate Circuits (MAC)
Week 13	Design of Digital Filters
Week 14	System Design of Neural Network
Week 15	FPGA with MATLAB
Week 16	**Final Exam**

Delivery Plan (Weekly Lab. Syllabus)

المنهاج الاسبوعي للمختبر

	Material Covered
Week 1	An introduction to the FPGA board - Vivado IDE
Week 2	VHDL code for Shift Register
Week 3	VHDL code for Multiplexer
Week 4	VHDL code for a counter
Week 5	VHDL code for SSD counter
Week 6	VHDL code for Full Adder
Week 7	VHDL code for Traffic Light Controller
Week 8	VHDL code for ALU
Week 9	VHDL code for Function and Procedure
Week 10	**Mid-Term Exam**
Week 11	VHDL code for MAC
Week 12	VHDL code for FIR Filter
Week 13	VHDL code for LPF Filter
Week 14	VHDL code for NN
Week 15	MATLAB to FPGA
Week 16	**Final Exam**

Learning and Teaching Resources

مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	Volnei A. Pedroni, "Circuit design with VHDL", MIT Press, 2004.	yes
Recommended Texts	Stephan Brown and Zvonko Vranesic , "Fundamentals of Digital Logic with VHDL Design", McGraw-Hill, 2000	no
Websites	https://nandland.com/fpga-101/	

Grading Scheme مخطط الدرجات				
Group	**Grade**	التقدير	**Marks %**	**Definition**
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.