MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Digital Circuits Design**			**Module Delivery**	
Module Type	**Core**			☒**Theory** ☒**Lecture** ☒**Lab** ☐**Tutorial** ☐**Practical** ☐**Seminar**	
Module Code	ATU11305				
ECTS Credits	**6**				
SWL (hr/sem)	**150**				
Module Level	UGII		**Semester of Delivery**	1	
Administering Department			**College**	NETC	
Module Leader	Huda Hussein Abed		**e-mail**	eng.huda2020@atu.edu.iq	
Module Leader's Acad. Title	Assistant Lecturer		**Module Leader's Qualification**	M.Sc.	
Module Tutor	Name (if available)		**e-mail**	E-mail	
Peer Reviewer Name	Nasir Hussein Selman		**e-mail**	Coj.nas@atu.edu.iq	
Scientific Committee Approval Date	01/10/2024		**Version Number**	1.0	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	1. Explain the concepts of sequential logic circuits. 2. Describe the difference between NAND and NOR latch. 3. Explain the operation of S-R, D, J-K, and T flip-flops. 4. Create the excitation table and characteristic equation for the flip-flops. 5. Design asynchronous counters and draw the timing diagram for them. 6. Define the modulus number for the counter. 7. Design synchronous counters and draw the timing diagram for them. 8. Explain the concepts of the shift register. 9. Implement the logic circuits of the multiplexer, demultiplexer, encoder, and decoder using logic gates.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Describe the difference between combinational logic circuits and sequential logic circuits. 2. Explain the operation of the S-R latch. 3. Identify the difference between a positive and a negative edge-triggered flip-flop. 4. Describe the outputs of a given flip-flop. 5. Explain the difference between asynchronous and synchronous counters. 6. Draw the timing diagram for the counters. 7. Design various types of counters according to the given requirement. 8. Write the modulus of the given counter and the entire count sequence. 9. Define the concept for cascading counters. 10. Explain the operation of a multiplexer and a demultiplexer. 11. Explain the operation of an encoder and a decoder.
Indicative Contents المحتويات الإرشادية	Indicative content includes the following. <u>Part A – Concept of sequential logic circuits and flip-flops</u> Define the sequential logic circuits, explain the operation of the S-R latch, determine the Q waveform for the NOR and NAND latch, define the flip-flop, explain the S-R, D, J-K, and T flip-flops, determine the Q output waveforms of the S-R, D, J-K, and T flip-flops, create the excitation table and characteristic equation for the flip- flops. [1-4 w] <u>Part B – Counters</u> Explain the operation of an asynchronous counter, design an asynchronous counter using J-K, D, and T flip-flops, draw the timing diagram for an asynchronous counter., define the modulus number for the counter, explain propagation delays in ripple counters, find the count sequence for the asynchronous counter with a truncated sequence, design of synchronous counters using J-K, T, and D flip-flops, analysis of synchronous counter to find the complete count sequence, create the timing diagram for the synchronous counter, describe the concept of cascading the counters, and explain the operation of a Johnson and Ring counters. [1-7 weeks] <u>Part C – Shift Registers</u>

	Describe the operation of four types of shift registers (SISO, SIPO, PISO, and PIPO), explain how data bits are entered into a shift register, and explain how data bits are taken out of a shift register. [1 week] Part D – Analysis and Design combinational logic circuits Implement 2:1, 4:1, and 8:1 multiplexers using logic gates, design higher order multiplexers using lower order multiplexers, implement logic functions using multiplexers, implement 1:2, 1:4, and 1:8 demultiplexers using logic gates, design higher order demultiplexers using lower order demultiplexers, describe the decimal-to-BCD encoder and the octal-to-binary encoder, explain the purpose of the priority feature in the binary encoders, describe the BCD-to-decimal decoder and the binary-to-octal decoder, and implement 2-to-4-line decoder with active low enable input using logic gates. [1-3 weeks]

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	• Interactive lecturing style, with opportunities for questions. • Encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. • Interactive simulation for the logic circuits. • Make tutorial questions for formative feedback. • Assessments related to students' answers are delivered with scientific comments.

Student Workload (SWL) الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	78	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	5.2
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	72	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	4.8
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	**150**		

Module Evaluation تقييم المادة الدراسية					
		Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**
Formative assessment	**Quizzes**	2	10% (10)	5 and 11	L #2, #3 and #8, #9
	Assignments	2	10% (10)	7 and 14	L #6, #7 and #13, #14
	Projects / Lab.	1	10% (10)	Continuous	All
	Report	1	10% (10)	13	LO #5, #10 and #12
Summative assessment	**Midterm Exam**	2hr	10% (10)	8	LO #1 - #7
	Final Exam	3hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري	
	Material Covered
Week 1	Introduction - Define the sequential logic circuits, and explain the operation of the S-R latch.
Week 2	Define the flip-flop, explain the operation of the S-R & D flip-flops, and determine the Q output waveforms of the S-R & D flip-flops.
Week 3	Explain the operation of J-K & T flip-flops, determine the Q output waveforms of the J-K & T flip-flops, and distinguish between synchronous and asynchronous inputs of the flip-flop.
Week 4	Create the excitation table of flip-flops, and derive the characteristic equation of the flip-flops.
Week 5	Design an asynchronous up binary counter using J-K flip-flops, design an asynchronous down binary counter using J-K flip-flops, and draw the timing diagram for an asynchronous counter.
Week 6	Describe the operation of an asynchronous up/down counter, define the modulus number for the counter, design a mod-10 asynchronous counter, and explain propagation delays in ripple counters.
Week 7	Design an asynchronous counter using D & T flip-flops, find the count sequence for the asynchronous counter with a truncated sequence, and explain the concept of frequency division.
Week 8	Mid-term Exam + Design of synchronous counters using J-K, T, and D flip-flops.
Week 9	Analysis of the synchronous counter to find the complete count sequence, create the timing diagram for the synchronous counter, and design a synchronous Up/Down counter.
Week 10	Design a synchronous decade counter, design a synchronous counter with the irregular count sequences, and describe the concept of cascading the counters.
Week 11	Explain the operation of a Johnson counter, draw the timing diagram for a Johnson counter, explain the operation of a ring counter, and draw the timing diagram for a Ring counter.

Week 12	Describe the operation of four types of shift registers (SISO, SIPO, PISO, and PIPO), explain how data bits are entered into a shift register, and explain how data bits are taken out of a shift register.
Week 13	Explain the basic operation of a multiplexer, implement 2:1, 4:1, and 8:1 multiplexers using logic gates, and design higher order multiplexers using lower order multiplexers.
Week 14	Implement logic functions using multiplexers, explain the basic operation of a demultiplexer, implement 1:2, 1:4, and 1:8 demultiplexers using logic gates, and design higher order demultiplexers using lower order demultiplexers.
Week 15	Describe the decimal-to-BCD encoder and the octal-to-binary encoder, explain the purpose of the priority feature in the binary encoders, describe the BCD-to-decimal decoder and the binary-to-octal decoder, and implement a 2-to-4-line decoder with active low enable input using logic gates.

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Lab 1: Implement the S-R latch using NOR gates & NAND gates.
Week 2	Lab 2: Construct S-R, and D flip-flops using logic gates.
Week 3	Lab 3: Construct J-K, and T flip-flops using logic gates.
Week 4	Lab 4: illustrate the effect of asynchronous inputs on the output of the J-K & D flip-flops
Week 5	Lab 5: Design an asynchronous up binary counter using J-K flip-flops.
Week 6	Lab 6: Design an asynchronous down binary counter using J-K flip-flops.
Week 7	Lab 7: Design a 4-bit synchronous counter using J-K flip-flops.
Week 8	Lab 8: Design a synchronous decade counter using J-K flip-flops.
Week 9	Lab 9: Design a Mod-8 Johnson counter using J-K flip-flops.
Week 10	Lab 10: Design a Mod-4 Ring counter using J-K flip-flops.
Week 11	Lab 11: Implement SISO shift register using J-K flip-flops.
Week 12	Lab 12: Implement a 4:1 multiplexer using logic gates.
Week 13	Lab 13: Implement a 1:4 demultiplexer using logic gates.
Week 14	Lab 14: Design a 4 to 2 encoder using logic gates.
Week 15	Lab 15: Design a 2-to-4-line decoder using logic gates.

Learning and Teaching Resources مصادر التعلم والتدريس		
	Text	**Available in the Library?**
Required Texts	1. G. K. Kharate, "Digital Electronics" Oxford university press, 7th edition, ISBN 13: 978-0-19-806183-0, 2013. 2. Thomas L. Floyd, "Digital Fundamentals" Pearson Education, 11th edition, ISBN 10: 1-292-07598-8, 2015. 3. T. Ndjountche "Digital Electronics 1", John Wiley & Sons, 1st edition, ISBN 978-1-84821-984-7, 2016. 4. N. S. Widmer, G. L. Moss, R. J. Tocci, "Digital Systems Principles and Applications", Pearson Education Limited e, 12th edition, ISBN 978-0-134-22013-0, 2017. 5. Shuqin Lou, Chunling Yang, "Digital Electronic Circuits" Science Press, 4th edition, ISBN 978-3-11-061466-4, 2019.	NO Yes Yes Yes NO
Recommended Texts	1. A. SAHA, and N. MANNA, "Digital Principles and Logic Design" Infinity science press LLC, ISBN: 978-1-934015-03-2, 2007. 2. M. M. Mano, and M. D. Ciletti "Digital Design" Pearson Education , 5th edition , ISBN-13: 978-0-13-277420-8, 2013.. 3. M. Rafiquzzaman, "Fundamentals of Digital Logic and Microcontrollers" John Wiley & Sons, Inc., 6th edition, ISBN 978-1-118-85579-9, 2014. 4. D. P. Kothari, and J. S. Dhillon "digital circuits and design" Pearson education, ISBN 978-93-325-4353-9, 2015. 5. Ata Elahi, "Computer Systems", Springer, ISBN 978-3-319-66774-4, 2018.	Yes Yes Yes No NO
Websites	https://www.allaboutcircuits.com/textbook/digital/ https://www.circuit-diagram.org/editor/ https://circuitverse.org/simulator	

Grading Scheme مخطط الدرجات				
Group	**Grade**	التقدير	**Marks %**	**Definition**
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.